IN THE CLAIMS:

Please amend the claims as follows. The claims are in the format as required by 35 C.F.R. § 1.121.

1. (Withdrawn) A semiconductor integrated circuit device comprising:

a semiconductor substrate having a first area;

a first counter provided in the first area, cyclically counting and outputting a first counter signal as a result of counting;

a global reset circuit provided on the semiconductor substrate and outputting a global reset signal;

a first local reset circuit provided in the first area and outputting a first local reset signal upon receiving the first counter signal of a set value after supplied with the global reset signal; and

a first circuit provided in the first area and supplied with the first local reset signal.

2. (Withdrawn) The device according to claim 1, wherein the semiconductor substrate has a second area, and

the device further comprises:

a second counter provided in the second area and counting a same value as the first counter at a same timing as first counter and outputting a second counter signal as a result of counting;

a second local reset circuit provided in the second area and outputting a second local reset signal upon receiving the second counter signal of the set value after supplied with the global reset signal; and

a second circuit provided in the second area and supplied with the second local reset signal.

3. (Withdrawn) The device according to claim 2, wherein the second area is located at a position which the global reset signal requires the longest time to reach, and

the set value is equal to a value counted by the first counter during time required by the global reset signal to reach the second area.

4. (Withdrawn) The device according to claim 2, wherein the first area is a range that the local reset signal from the local reset circuit travels before the first counter counts 1.

5. (Withdrawn) The device according to claim 1, further comprising:

a clock source outputting a clock signal;

a plurality of buffers each of which is supplied by the clock source with the clock signal via a signal line which communicates a signal within one cycle of the clock signal and each of which distributes the clock signal to a plurality of areas including the first area via a signal line which communicates a signal within one cycle of the clock signal, and

wherein the first counter counts in synchronism with the clock signal supplied by the buffer.

6. (Currently Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate having a first area and a second area;

a plurality of counters one of which is provided in the first area and the second area and which cyclically count a same value at a same timing in synchronism with a first clock signal and output a counter signal as a result of counting;

a first clock circuit provided in the first area, supplied with ~~the~~ a first counter signal from the one of the counters in the first area and outputting a second clock signal having a phase which becomes zero every time the first counter signal counts n times (n being a natural number);

a first circuit provided in the first area and operating in synchronism with the second clock signal;

a second clock circuit provided in the second area, supplied with ~~the~~ a second counter signal from the one of the counters in the second area and outputting a third clock signal having a phase which becomes zero every time the second counter signal counts m times (m being a natural number different from n); and

a second circuit provided in the second area, operating in synchronism with the third clock signal and supplying the first circuit with data when the first and second counter signals ~~has~~ have a value equal to a common multiple of n and m.

7. (Original) The device according to claim 6, wherein the first area is equal to a range that the second clock signal from the first clock circuit travels within one cycle of the first clock signal.

8. (Original) The device according to claim 6, further comprising:

a clock source outputting a clock signal;

a plurality of buffers each of which is supplied by the clock source with the clock signal via a signal line which communicates a signal within one cycle of the clock signal and each of which distributes the clock signal to a plurality of areas including the first area and the second area via a signal line which communicates a signal within one cycle of the clock signal, and

wherein the plurality of counters count in synchronism with the clock signal supplied by the buffer.

9. (Currently Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate having a first area and a second area;

a plurality of counters one of which is provided in the first area and the second area and

which cyclically count a same value at a same timing and output a counter signal as a result of counting;

a first circuit provided in the first area, supplied with ~~the~~ a first counter signal from the one of the counters in the first area and outputting a first signal when the first counter signal has a first value; and

a second circuit provided in the second area, supplied with ~~the~~ a second counter signal from the one of the counters in the second area and supplying the first circuit with a second signal containing information on a value of the second counter signal obtained upon reception of the first signal.

10. (Currently Amended) The device according to claim 9, wherein the semiconductor substrate has a third area in which one of the plurality of counters is provided,

the semiconductor integrated circuit device further comprises a third circuit provided in the third area, supplied with ~~the~~ a third counter signal from the one of the counters in the third area and supplying the first circuit with a third signal containing information on a value of the third counter signal obtained upon reception of the first signal,

the second circuit outputs a fourth signal when the second counter signal has a second value,

the first circuit supplies the second circuit with a fifth signal containing information on a value of the first counter signal obtained upon reception of the fourth signal, and

the third circuit supplies the second circuit with a sixth signal containing information on a value of the third counter signal obtained upon reception of the fourth signal.

11. (Withdrawn) A semiconductor integrated circuit device comprising:

a semiconductor substrate having a first area and a second area;

a first counter provided in the second area, cyclically counting in synchronism with the

first clock signal and outputting a first counter signal as a result of counting;

a first clock circuit supplied with the first counter signal and the first clock signal and outputting a second clock signal having a phase which becomes zero when supplied with the first counter signal with a value of n (n being a natural number) and the first clock signal in a first state; and

a first circuit provided in the second area and operating in synchronism with the second clock signal.

12. (Withdrawn) The device according to claim 11, wherein the semiconductor substrate has a third area, and

the semiconductor integrated circuit device further comprises:

a second counter provided in the third area, cyclically counting at a same timing as the first counter signal and outputting a second counter signal as a result of counting;

a second clock circuit supplied with the second counter signal and the first clock signal and outputting a third clock signal having a phase which becomes zero when supplied with the second counter signal with a value of m (m being a natural number) and the first clock signal in the first state; and

a second circuit provided in the third area and operating in synchronism with the third clock signal.

13. (Withdrawn) The device according to claim 12, wherein the first counter counts the same value as that counted by the second counter,

m is equal to n, and

the second clock signal and the third clock signal have different phases.

14. (Withdrawn) The device according to claim 11, wherein the first area is a range that the second clock signal from the first clock circuit travels within one cycle of the first clock signal.

15. (Withdrawn) The device according to claim 11, further comprising:

a clock source outputting a clock signal;

a plurality of buffers each of which is supplied by the clock source with the clock signal via a signal line which communicates a signal within one cycle of the clock signal and each of which distributes the clock signal to a plurality of areas including the first area and the second area via a signal line which communicates a signal within one cycle of the clock signal, and

wherein the first counter counts in synchronism with the clock signal supplied by the buffer.

16. (Withdrawn) The device according to claim 11, wherein the first counter and the second counter count different values during a same cycle.

17. (Withdrawn) The device according to claim 16, wherein the first area is a range that the second clock signal from the first clock circuit travels within one cycle of the first clock signal.

18. (Withdrawn) The device according to claim 11, wherein the first counter has at least one of a function for continuously supplying the first counter signal of a same value, a function for selecting supply or stoppage of the first counter signal, and a function for starting counting with a certain value.

19. (Withdrawn) The device according to claim 18, wherein the first area is a range that the second clock signal from the first clock circuit travels within one cycle of the first clock signal.

20. (Withdrawn) A method of outputting signals on semiconductor integrated circuit comprising:

outputting a first counter signal as a result of cyclic counting from a first counter provided in a first area on a semiconductor substrate;

outputting a global reset signal from a global reset circuit provided on the semiconductor substrate;

outputting a first local reset signal from a first local reset circuit provided in the first area to a first circuit provided in the first area when the first local reset circuit receives the first counter signal of a set value after supplied with the global reset signal.